07-25-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UTILITY PATENT APPLICATION TRANSMITTAL LETTER

Attorney Docket No.: JG00009
Mailing Date: July 24, 2000
Express Mail EL568745641US

To: Assistant Commissioner for Patents
Box Patent Application
Washington D.C., 20231

Dear Sir:

Transmitted herewith for filing under 37 C.F.R. 1.53(b) is a:

☒ New Nonprovisional Utility Patent Application; or

☐ Continuation; or ☐ Divisional; or ☐ Continuation-In-Part (CIP); of prior US Application No. _____, filed on _____, having U.S. Examiner _____, in Group Art Unit _____

Of: Nada El-Zein, Jamal Ramdani, Kurt Eisenbeiser, and Ravindranath Droopad

For: **HETEROJUNCTION TUNNELING DIODES AND PROCESS FOR FABRICATING SAME**

☒ 7 sheets of drawings and 60 pages of specification and claims.

☒ Newly executed oath or declaration combined with Power of Attorney on 2 pages.

☐ Copy of oath or declaration from prior U.S. application serial no._____
☐ The following named inventor(s) from the prior application are hereby deleted from this application in accordance with 37 C.F.R. 1.63(d)(2) and 1.33(b): _____.

☐ Foreign priority to EPO patent application having serial number_____ and a filing date of _____, is hereby claimed under 35 USC 119.

☒ An Assignment Transmittal Letter and Assignment of the invention to Motorola, Inc.

☒ An Information Disclosure Statement (IDS), with PTO-1449, and 28 citation copies.

☒ Return Receipt Postcard.

☐ Preliminary Amendment.

☐ Please cancel pending claims _____.

☐ Incorporation by Reference (for Continuation/Division/CIP application). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. Since the present application is based on a prior US application, please amend the specification by adding the following sentence before the first sentence of the specification:

"The present application is based on prior US application No._____, filed on_____ _____, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed."

☐ Applicant hereby petitions pursuant to 37 C.F.R. §1.136(a) for a _____ month extension of time for response to the outstanding Official Action mailed_____. The period for response was previously set to elapse _____, and is accordingly hereby extended to _ __, which is still within the six-month statutory period for response (35 U.S.C. § 133) which elapses _____. The reason for this petition is that a Division, Continuation, or CIP is being filed, and it is desired to maintain the present application in pending condition pursuant to 35 USC § 120 through at least the filing of the Division, Continuation, or CIP application. The required Extension Fee established by 37 C.F.R. § 1.17(a) pursuant to 35 U.S.C. § 41(a) (8) is:

EXTENSION	FEE
☐ First Month	$110.00
☐ Second Month	$380.00
☐ Third Month	$870.00
☐ Fourth Month	$1,360.00
☐ Fifth Month	$1,850.00

☒ The filing fee is calculated as follows:

CLAIMS AS FILED, LESS ANY CANCELED BY AMENDMENT

FOR	NUMBER OF CLAIMS	NUMBER EXTRA	RATE	FEE
TOTAL CLAIMS	60 - 20 =	40	x $18	= $ 720.00
INDEPENDENT CLAIMS	4 - 3 =	2	x $78	= $ 156.00
MULTIPLE DEPENDENT CLAIMS			$260	= $ 0.00
BASIC FEE				= $ 690.00
TOTAL FILING FEE				= $ 1566.00

☒ Please charge Deposit Account No. 13-4771 in the amount of $ 1566.00 for the Total Filing Fee, and the Extension Fee under 37 C.F.R. §1.136(a), if applicable.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required now or in the future during the entire pendency of this application under 37 C.F.R. 1.16 or 37 C.F.R. 1.17, including any present or future time extension fees which may be required, or credit any overpayment to Deposit Account No. 13-4771.

☒ This sheet is submitted in duplicate.

This transmittal letter has 2 total pages.

24 July 2010
DATE

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HETEROJUNCTION TUNNELING DIODES AND PROCESS FOR FABRICATING SAME

Field of the Invention

This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to the fabrication and use of resonant heterojunction tunnel diodes that include a monocrystalline compound semiconductor material.

Background of the Invention

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the so-called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that make these materials advantageous for certain types of semiconductor devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most readily available compound semiconductor material, is available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of the compound semiconductor material, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure, such as, for example, a resonant heterojunction tunnel diode, could be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

Tunnel diodes, where carriers tunnel through the band gap of a doped p-n junction, have taken many forms since first proposed in about 1958. Tunnel diodes provide very fast switching time and low power dissipation. The first

tunnel diode, called an Esaki tunneling diode (after its originator), comprised two silicon regions of different conductivity types with both being highly doped. When bias is applied to the Esaki-type diode, the available states for electrons in the contact layer align with available states for holes in the valence band of the injection layer and tunneling occurs. Traditional Esaki diodes formed in silicon-based material systems, however, exhibit low peak current densities, low peak-to-valley current ratios, and low operational frequencies, which make them unsuitable for present-day demands for enhanced performance in areas such as high frequency circuits, portable communications systems, and digital applications. Thus, present-day Esaki-type diodes may comprise germanium, gallium arsenide, or other semiconductor materials, which exhibit more suitable electrical properties. For example, tunnel diodes having the most favorable electrical properties are currently manufactured in compound semiconductor material systems comprising materials such as indium aluminum arsenide (InAlAs), indium gallium arsenide (InGaAs), indium phosphide (InP), gallium arsenide (GaAs), and aluminum arsenide (AlAs). Unfortunately, as stated above, such compound semiconductor substrates tend to be expensive and extremely fragile.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film over another monocrystalline material and for a process for making such a structure.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in

which like references indicate similar elements, and in which:

FIGS. 1 - 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer;

FIG. 9 illustrates schematically, in cross section, a monolithic integrated circuit in accordance with one embodiment of the invention; and

FIGS. 10-17 illustrate schematically, in cross section, device structures in accordance with further exemplary embodiments of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and

preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and/or to the subsequently applied semiconductor

material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs),

gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner

to that described above. Monocrystalline semiconductor layer 38 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38

is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the

application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic

phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2

monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and

preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as

described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and Sr_zBa_{1-z} TiO_3 (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal

orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that has a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of

the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host

material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate,

although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the

reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stoichiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound

semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the

accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or ``conventional'' thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26 may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor

layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with

the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 illustrates schematically, in cross section, a device structure 900 in accordance with a further embodiment of the invention. Device structure 900 includes a monocrystalline semiconductor substrate 901, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 901 includes two regions, 902 and 903. An electrical semiconductor component generally indicated by the dashed line 909 is formed in region 902. Electrical component 909 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated circuit such as a MOS integrated circuit. For example, electrical component 909 can be a MOS circuit configured to perform digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 902 can be

formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 904 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 909.

Insulating material 904 and any other layers that may have been formed or deposited during the processing of semiconductor component 909 in region 902 are removed from the surface of region 903 to provide a bare substrate surface in that region, for example, a bare silicon surface. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. A layer of barium or barium and oxygen may be deposited onto the native oxide layer on the surface of region 903 and then reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment of the invention, a monocrystalline oxide layer 906 is formed overlying the template layer by a process of molecular beam epitaxy. In one aspect of this exemplary embodiment, reactants including barium, titanium, and oxygen are deposited onto the template layer to form the monocrystalline oxide layer. Initially during the deposition, the partial pressure of oxygen is kept near the minimum necessary to fully react with the barium and titanium to form a monocrystalline barium titanate layer 906. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the barium titanate reacts with silicon at the surface of region 903 to form an amorphous layer 905 is silicon oxide on the second region and at the interface between the silicon substrate and the monocrystalline oxide.

In accordance with an embodiment of the invention, the step of depositing the monocrystalline oxide layer 906 is followed by depositing a second template layer (not shown), which can be 1-10 monolayers of titanium, barium, strontium, barium and oxygen, titanium and oxygen, or strontium and oxygen. A buffer layer 907 of a monocrystalline semiconductor material is then deposited overlying the second template layer by a process of molecular beam epitaxy. The deposition of buffer layer 907 may be initiated, for example, by depositing a layer of arsenic onto the template. This initial step is then followed by depositing gallium and arsenic to form monocrystalline gallium arsenide. Alternatively, strontium may be substituted for barium in the above example. Further, layer 907 may comprise any suitable monocrystalline semiconductor material, as described herein.

In accordance with one aspect of the present embodiment, after monocrystalline oxide layer 906 formation, the monocrystalline titanate layer and the silicon oxide layer, which is interposed between substrate 901 and the titanate layer, are exposed to an anneal process such that the titanate and oxide layers form an amorphous oxide layer 905. An additional compound semiconductor layer 908 is then epitaxially grown over layer 907, using the techniques described above in connection with layer 907. Alternatively, the above-described anneal process can be performed after formation of additional compound semiconductor layer 908.

In accordance with a further embodiment of the invention, a semiconductor component, generally indicated by a dashed line 910, is formed in compound semiconductor layer 908. Semiconductor component 910 can be formed by processing steps conventionally used in the fabrication of

gallium arsenide or other III-V compound semiconductor material devices. Semiconductor component 910 may be any active or passive component, and preferably is a tunneling diode, light emitting diode, semiconductor laser, photodetector, heterojunction bipolar transistor (HBT), high frequency MESFET, or other component that utilizes and takes advantage of the physical properties of compound semiconductor materials. A metallic conductor schematically indicated by the line 911 can be formed to electrically couple device 910 and device 909, thus implementing an integrated device that includes at least one component formed in the silicon substrate and one device formed in the monocrystalline semiconductor material layer. Although illustrative structure 900 has been described as a structure formed on a silicon substrate 901 and having a barium (or strontium) titanate layer 906 and a gallium arsenide layer 908, similar devices can be fabricated using other monocrystalline substrates, monocrystalline oxide layers and other monocrystalline compound semiconductor layers as described elsewhere in this disclosure.

FIG. 10 illustrates a semiconductor structure 1000 in accordance with a further embodiment of the invention. In this embodiment, structure 1000 is a resonant interband tunnel diode formed of monocrystalline epitaxial layers of compound semiconductor material on a monocrystalline silicon substrate. Structure 1000 includes a monocrystalline semiconductor substrate 1001, such as a monocrystalline silicon wafer. An amorphous oxide layer 1002 is preferably formed overlying substrate 1001, in accordance with the process described above. An accommodating buffer layer 1003 is formed overlying substrate 1001 and amorphous oxide layer 1002. As described above, amorphous oxide layer 1002 may be grown

at the interface between substrate 1001 and the growing accommodating buffer layer 1003 by the oxidation of substrate 1001 during the growing of layer 1003. Accommodating buffer layer 1003 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. In this embodiment, wherein substrate 1001 is monocrystalline silicon and the overlying compound semiconductor material layer is monocrystalline GaAs, layer 1003 may comprise, for example, an alkali earth metal titanate such as barium titanate or strontium titanate.

An additional buffer layer 1004 is preferably formed overlying layer 1003 to alleviate any strains that might result from a mismatch of the crystal lattice of accommodating buffer layer 1003 and the lattice of the monocrystalline semiconductor material layer. In this exemplary embodiment, buffer layer 1004 is a layer of GaAs and can have a thickness of about 500 to about 2000 nanometers (nm) and preferably a thickness of about 500 to about 1000 nm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide on the monocrystalline oxide, a template layer (not shown) may be formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O.

In accordance with this embodiment of the invention, carrier supply layer 1005 is a layer of n+ doped GaAs having a thickness of about 500 nanometers (nm). A first quantum well layer 1006, a barrier layer 1007, and a second quantum well layer 1008 are epitaxially grown, in succession, on carrier supply layer 1005. In accordance

with this embodiment of the invention, quantum well layers 1006 and 1008 are layers of indium gallium arsenide (InGaAs) having a thickness of about 4 to about 5 nanometers (nm). Barrier layer 1007 is a layer of GaAs having a thickness of about 2 to about 4 nanometers (nm). Quantum well layers 1006, 1008 and barrier layer 1007 are not intentionally doped. After formation of layers 1006, 1007, and 1008, a second carrier supply layer 1009 is grown on second quantum well layer 1008. In accordance with this embodiment of the invention, carrier supply layer 1009 is a layer of p+ doped GaAs having a thickness of about 50 nanometers (nm).

FIG. 11 illustrates a semiconductor structure 1100 in accordance with a further embodiment of the invention. In this embodiment, structure 1100 is a resonant interband tunnel diode formed of monocrystalline epitaxial layers of compound semiconductor material on a monocrystalline silicon substrate. Structure 1100 includes a monocrystalline semiconductor substrate 1101, such as a monocrystalline silicon wafer. An amorphous oxide layer 1102 is preferably formed overlying substrate 1101, in accordance with the process described above. An accommodating buffer layer 1103 is formed overlying substrate 1101 and amorphous oxide layer 1102. As described above, amorphous oxide layer 1102 may be grown at the interface between substrate 1101 and the growing accommodating buffer layer 1103 by the oxidation of substrate 1101 during the growing of layer 1103. Accommodating buffer layer 1103 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. In this embodiment, wherein substrate 1101 is monocrystalline silicon and the overlying compound

semiconductor material layer is monocrystalline InP, layer 1103 may comprise, for example, an alkali earth metal zirconate such as strontium zirconate or barium zirconate, or an alkali earth metal hafnate such as strontium hafnate or barium hafnate.

An additional buffer layer 1104 is preferably formed overlying layer 1103 to alleviate any strains that might result from a mismatch of the crystal lattice of accommodating buffer layer 1103 and the lattice of the monocrystalline semiconductor material layer. In this exemplary embodiment, buffer layer 1104 is a layer of InP or indium aluminum arsenide (InAlAs) and can have a thickness of about 50 nanometers (nm). To facilitate the epitaxial growth of the InP or InAlAs on the monocrystalline oxide, a template layer (not shown) may be formed by capping the oxide layer. The template layer may be 1-10 monolayers of Zr-As, Hf-As, Zr-P, Hf-P, Sr-O-As, Sr-O-P, Ba-O-As, Ba-O-P, or In-Sr-O. For example, where layer 1103 is barium zirconate, the template layer may be 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template.

In accordance with this embodiment of the invention, a first carrier supply layer having first and second layers 1105 and 1106 of doped monocrystalline semiconductor material is formed overlying buffer layer 1104. Layers 1105 and 1106 are n+ doped InGaAs having a thickness of about 50 to about 100 nanometers (nm) and n+ doped InAlAs having a thickness of about 50 to about 100 nm, respectively. If tunnel diode structure 1100 is later electrically coupled to a second semiconductor device, layer 1105 may serve as a contact layer for the electrical interconnects.

A first quantum well layer 1107, a barrier layer 1108, and a second quantum well layer 1109 are epitaxially

grown, in succession, on carrier supply layer 1106. In accordance with this embodiment of the invention, quantum well layers 1107 and 1109 are layers of InGaAs having a thickness of about 4 nm. Barrier layer 1108 is a layer of InAlAs having a thickness of about 2 nm. Quantum well layers 1107, 1109 and barrier layer 1108 are not intentionally doped. After formation of layers 1107, 1108 and 1109, a second carrier supply layer having first and second layers 1110 and 1111 of doped monocrystalline semiconductor material is grown on second quantum well layer 1109. Layers 1110 and 1111 are p+ doped InAlAs having a thickness of about 50 to about 100 nanometers (nm) followed by a p+ doped InGaAs layer having a thickness of about 50 to about 100 nm. If tunnel diode structure 1100 is later electrically coupled to a second semiconductor device, layer 1111 may serve as a contact layer for the electrical interconnects.

FIG. 12 illustrates a semiconductor structure 1200 in accordance with a further embodiment of the invention. In this embodiment, structure 1200 is a resonant intraband tunnel diode formed of monocrystalline epitaxial layers of compound semiconductor material on a monocrystalline silicon substrate. Structure 1200 includes a monocrystalline semiconductor substrate 1201, such as a monocrystalline silicon wafer. An amorphous oxide layer 1202 is preferably formed overlying substrate 1201, in accordance with the process described above. An accommodating buffer layer 1203 is formed overlying substrate 1201 and amorphous oxide layer 1202. As described above, amorphous oxide layer 1202 may be grown at the interface between substrate 1201 and the growing accommodating buffer layer 1203 by the oxidation of substrate 1201 during the growing of layer 1203. Accommodating buffer layer 1203 is preferably a

monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. In this embodiment, wherein substrate 1201 is monocrystalline silicon and the overlying compound semiconductor material layer is monocrystalline GaAs, layer 1203 may comprise, for example, an alkali earth metal titanate such as barium titanate or strontium titanate.

An additional buffer layer 1204 is preferably formed overlying layer 1203 to alleviate any strains that might result from a mismatch of the crystal lattice of accommodating buffer layer 1203 and the lattice of the monocrystalline semiconductor material layer. In this exemplary embodiment, buffer layer 1204 is a layer of GaAs and can have a thickness of about 500 to about 2000 of about 50 to about 100 nanometers (nm) and preferably a thickness of about 500 to about 1000 nm. To facilitate the epitaxial growth of the gallium arsenide on the monocrystalline oxide, a template layer (not shown) may be formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O.

In accordance with a preferred embodiment of the invention, a first contact layer 1205 is formed on buffer layer 1204 and comprises a layer of n+ doped GaAs having a thickness of about 50 nm. A collection layer 1206 is then formed overlying contact layer 1205, and comprises a layer of n- doped GaAs having a thickness of about 50 nm.

Following formation of collection layer 1206, a first tunnel barrier layer 1207, a quantum well layer 1208, and a second tunnel barrier layer 1209 are epitaxially grown, in succession, on the collection layer. In accordance with this embodiment of the invention, tunnel barrier

layers 1207 and 1209 are layers of aluminum gallium arsenide (AlGaAs) or aluminum arsenide (AlAs) having a thickness of about 5 nm. Quantum well layer 1208 is a layer of GaAs having a thickness of about 5 nm. Quantum well layer 1208 and tunnel barrier layers 1207 and 1209 are not intentionally doped. After formation of layers 1207, 1208, and 1209, an injection layer 1210 is grown on second tunnel barrier layer 1209. In accordance with this embodiment of the invention, injection layer 1210 is a spacer layer of n^- doped GaAs having a thickness of about 50 nm. In accordance with a preferred embodiment of the invention, a second contact layer 1211 is formed on injection layer 1210 and comprises a layer of n+ doped GaAs having a thickness of about 50 nm.

FIG. 13 illustrates a semiconductor structure 1300 in accordance with a further embodiment of the invention. In this embodiment, structure 1300 is a resonant intraband tunnel diode formed of monocrystalline epitaxial layers of compound semiconductor material on a monocrystalline silicon substrate. Structure 1300 includes a monocrystalline semiconductor substrate 1301, such as a monocrystalline silicon wafer. An amorphous oxide layer 1302 is preferably formed overlying substrate 1301, in accordance with the process described above. An accommodating buffer layer 1303 is formed overlying substrate 1301 and amorphous oxide layer 1302. As described above, amorphous oxide layer 1302 may be grown at the interface between substrate 1301 and the growing accommodating buffer layer 1303 by the oxidation of substrate 1301 during the growing of layer 1303. Accommodating buffer layer 1303 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material.

In this embodiment, wherein substrate 1301 is monocrystalline silicon and the overlying compound semiconductor material layer is monocrystalline InP, layer 1303 may comprise, for example, an alkali earth metal zirconate such as strontium zirconate or barium zirconate, or an alkali earth metal hafnate such as strontium hafnate or barium hafnate.

An additional buffer layer 1304 is preferably formed overlying layer 1303 to alleviate any strains that might result from a mismatch of the crystal lattice of accommodating buffer layer 1303 and the lattice of the monocrystalline semiconductor material layer. In this exemplary embodiment, buffer layer 1304 is a layer of InP or InAlAs and can have a thickness of about 500 to about 2000 nanometers (nm) and preferably a thickness of about 500 to about 1000 nm. To facilitate the epitaxial growth of the InP or InAlAs on the monocrystalline oxide, a template layer (not shown) may be formed by capping the oxide layer. The template layer may be 1-10 monolayers of Zr-As, Hf-As, Zr-P, Hf-P, Sr-O-As, Sr-O-P, Ba-O-As, Ba-O-P, or In-Sr-O. For example, where layer 1303 is barium zirconate, the template layer may be 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template.

In accordance with a preferred embodiment of the invention, a first contact layer 1305 is formed on buffer layer 1304 and comprises a layer of n+ doped InGaAs having a thickness of about 50 nm. A spacer layer 1306 is then formed overlying contact layer 1305, and comprises a layer of InGaAs having a thickness of about 50 nm.

Following formation of spacer layer 1306, a first tunnel barrier layer 1307, a quantum well layer 1308, and a second tunnel barrier layer 1309 are epitaxially grown, in succession, on the spacer layer. In accordance with

this embodiment of the invention, tunnel barrier layers 1307 and 1309 are layers of AlAs or InAlAs having a thickness of about 5 nm. Quantum well layer 1308 is a layer of InGaAs having a thickness of about 5 nm. Quantum well layer 1308 and tunnel barrier layers 1307 and 1309 are not intentionally doped. After formation of layers 1307, 1308, and 1309, a spacer layer 1310 is grown on second tunnel barrier layer 1309. In accordance with this embodiment of the invention, spacer layer 1310 is a layer of n- InGaAs having a thickness of about 5 nm. Preferably, injection layer 1310 is not intentionally doped. In accordance with a preferred embodiment of the invention, a contact layer 1311 is formed overlying injection layer 1310 and comprises n+ doped InGaAs having a thickness of about 50 nm..

Referring now to FIG. 14, a monolithic integrated circuit is provided in accordance with one embodiment of the present invention. Monolithic integrated circuit 1400 generally includes a MOS circuit 1401 electrically coupled to a tunnel diode. In FIG. 14, for illustration purposes only, and without limitation, MOS circuit 1401 is electrically coupled to an intraband tunnel diode 1300, such as that exhibited in FIG. 13. Composite layers 1302 through 1311, as presented in FIG. 14, are identical to those illustrated and described above with reference to FIG. 13. In this embodiment, semiconductor substrate 1301 is a monocrystalline silicon substrate, such as a silicon wafer.

In accordance with the present embodiment of the invention, MOS circuit 1401 is first formed in semiconductor substrate 1301 using conventional processing steps and techniques well known to those skilled in the art. MOS circuit 1401 generally comprises a gate electrode 1402, a gate dielectric layer 1403, and n+ doped

regions 1404. Gate dielectric layer 1403 is formed over a portion of substrate 1301, and gate electrode 1402 is then formed over gate dielectric layer 1403. Selective n-type doping is performed to form n+ doped regions 1404 within substrate 1301 along adjacent sides of gate electrode 1402 and are source, drain, or source/drain regions for the MOS transistor. The n+ doped regions 1404 have a doping concentration of at least about 1E19 atoms per cubic centimeter to allow one or more ohmic contacts to be formed. In this embodiment, n+ doped region 1404 is a drain region for the MOS transistor. After formation of MOS portion 1401 of the integrated circuit, all of the layers formed during processing are removed from the surface of substrate 1301 in the region where tunnel diode 1300 will be formed. A bare silicon surface is thus provided for the subsequent processing of tunnel diode 1300, for example in the manner set forth above.

After formation of both MOS circuit 1401 and tunnel diode 1300 on substrate 1301, processing continues to form a substantially completed integrated circuit 1400. Ohmic contacts 1405 and 1406 may be formed on drain region 1404 and contact layer 1312, respectively, using standard processing techniques well known in the art. An insulating layer 1408 is formed over substrate 1301, MOS circuit 1401, and tunnel diode 1300. Portions of insulating layer 1408 are then removed to define contact openings where the devices are to be interconnected. Interconnect trenches are formed within insulating layer 1408 to provide the lateral connections between the contacts. As illustrated in FIG. 14, interconnect 1407 connects a drain region of the MOS circuit to the uppermost contact layer 1312 of tunnel diode 1300. A passivation layer 1409 is formed over the interconnect 1407 and insulating layer 1408. Other electrical

connections may be made to the devices and/or other electrical or electronic components within the integrated circuit 1400 but not illustrated in the figure according to conventional techniques available to those skilled in the art.

Referring now to FIG. 15, a monolithic integrated circuit is provided in accordance with one embodiment of the present invention. Monolithic integrated circuit 1500 generally includes a MOS circuit 1401 electrically coupled in series to first and second tunnel diodes. In FIG. 15, for illustration purposes only, and without limitation, MOS circuit 1401 is electrically coupled to first and second intraband tunnel diodes 1200 and 1501 of the type illustrated and described with reference to FIG. 12. Composite layers 1202 through 1210, as presented in FIG. 15, are identical to those illustrated and described above with reference to FIG. 12. In this embodiment, semiconductor substrate 1201 is a monocrystalline silicon substrate, such as a silicon wafer.

In accordance with the present embodiment of the invention, MOS circuit 1401 is first formed in semiconductor substrate 1301 using conventional processing steps and techniques well known to those skilled in the art, in accordance with the above description in reference to FIG. 14. First tunnel diode 1200 is formed in accordance with FIG. 12 and its accompanying description, except that second contact layer 1211 is omitted, leaving injection layer 1210 as the top layer of first tunnel diode 1200.

Second tunnel diode 1501 is formed overlying injection layer 1210 of first tunnel diode 1200, beginning with formation of a collection layer 1506. In the present embodiment of the invention, collection layer 1506 is a layer of n-doped GaAs. Following formation of collection

layer 1506, a first tunnel barrier layer 1507, a quantum well layer 1508, and a second tunnel barrier layer 1509 are grown, in succession, on the collection layer. In accordance with this embodiment of the invention, tunnel barrier layers 1507 and 1509 are layers of AlGaAs or AlAs. Quantum well layer 1508 is a layer of GaAs. Quantum well layer 1508 and tunnel barrier layers 1507 and 1509 are not intentionally doped. After formation of layers 1507, 1508, and 1509, a spacer layer 1510 comprising n^- doped GaAs is grown on second tunnel barrier layer 1509. Finally, a contact layer 1511 is formed on spacer layer 1510 and comprises a layer of n+ doped GaAs.

As detailed with reference to FIG. 14, after formation of both MOS circuit 1401 and tunnel diodes 1200 and 1501 on substrate 1301, processing continues to form a substantially completed integrated circuit 1500. Ohmic contacts 1405 and 1406 may be formed on drain region 1404 and contact layer 1512, respectively. An insulating layer 1408 is formed over substrate 1301, MOS circuit 1401, and tunnel diodes 1200 and 1501. Portions of insulating layer 1408 are then removed to define contact openings where the devices are to be interconnected. Interconnect trenches are formed within insulating layer 1408 to provide the lateral connections between the contacts. As illustrated in FIG. 15, interconnect 1407 connects a drain region of the MOS circuit to the uppermost contact layer 1512 of tunnel diode 1501. A passivation layer 1409 is formed over the interconnect 1407 and insulating layer 1408. Other electrical connections may be made to the devices and/or other electrical or electronic components within the integrated circuit 1500 (not illustrated in the figure) according to conventional techniques available to those skilled in the art.

Referring now to FIG. 16, a monolithic integrated circuit is provided in accordance with one embodiment of the present invention. Monolithic integrated circuit 1600 generally includes a MOS circuit 1401 having a drain region 1604 and a tunnel diode 1300 formed overlying and electrically coupled to the drain region. In FIG. 16, for illustration purposes only, and without limitation, MOS circuit 1401 is electrically coupled to an intraband tunnel diode 1300 of the type illustrated and described with reference to FIG. 13. Composite layers 1303 through 1311, as presented in FIG. 16, are identical to those illustrated and described above with reference to FIG. 13. In this embodiment, semiconductor substrate 1301 is a monocrystalline silicon substrate, such as a silicon wafer.

In this embodiment, no amorphous layer is formed between substrate 1301 and monocrystalline layer 1303. Rather, monocrystalline oxide layer 1303 is formed overlying drain region 1604 and is selectively doped to render the oxide electrically conductive. Intraband tunnel diode 1300 is then formed in accordance with the above description in electrical contact with the electrically conductive oxide of layer 1303.

In FIG. 17, a monolithic integrated circuit 1700 generally includes a MOS transistor having a gate electrode and a tunnel diode formed overlying and electrically coupled to the gate electrode. In FIG. 17, for illustration purposes only, and without limitation, an interband tunnel diode generally of the type illustrated and described with reference to FIG. 10 is formed overlying the gate electrode of the MOS transistor. In this embodiment, semiconductor substrate 1701 is a monocrystalline silicon substrate, such as a silicon wafer. N+ doped regions 1702 represent the source, drain,

or source/drain regions of the MOS transistor, and are formed via ion implantation in substrate 1701.

An amorphous oxide layer 1709 is preferably formed overlying substrate 1701, in accordance with the process described above. In accordance with this embodiment of the present invention, a monocrystalline oxide layer 1703 is formed overlying amorphous layer 1709. Gate electrode 1704 is then formed overlying monocrystalline oxide layer 1703 in accordance with the above-described techniques. In this embodiment, gate electrode 1704 is a layer of n+ doped GaAs and can have a thickness of about 50 to about 500 nanometers (nm) and preferably a thickness of about 50 to about 100 nm.

A first quantum well layer 1705, a barrier layer 1706, and a second quantum well layer 1707 are grown, in succession, on gate electrode 1704. In accordance with this embodiment of the invention, quantum well layers 1705 and 1707 are InGaAs and barrier layer 1706 is GaAs, none of which are intentionally doped. After formation of layers 1705, 1706, and 1707, a p+ doped GaAs carrier supply layer 1708 is epitaxially grown on second quantum well layer 1707.

Clearly, these embodiments of integrated circuits having compound semiconductor portions and Group IV semiconductor portions are meant to illustrate embodiments of the present invention and do not limit the present invention. There are a multiplicity of other combinations of semiconductor devices and other embodiments of the present invention that come within the present disclosure. For example, the compound semiconductor portion may include light emitting diodes, photodetectors, diodes, or the like, and the Group IV semiconductor portions can include digital logic, memory arrays, and most structures that can be formed in conventional MOS integrated

circuits. By using embodiments of the present invention, it is now simpler to integrate devices that work better in compound semiconductor materials with other components that work better or are easily and/or inexpensively formed within Group IV semiconductor materials. This allows the device size to decrease, the manufacturing costs to decrease, and yield and reliability to increase.

As contemplated in the above description, a monocrystalline Group IV wafer can also be used in forming only compound semiconductor electrical components over the wafer. In this manner, the wafer is essentially a ``handle'' wafer used during the fabrication of the compound semiconductor electrical components within a monocrystalline compound semiconductor layer overlying the wafer. Therefore, electrical components can be formed within II-V or II-IV semiconductor materials over a wafer of at least approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive ``handle'' wafer overcomes the fragile nature of the compound semiconductor wafers by placing them over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within the compound semiconductor material even though the substrate itself may include a Group IV semiconductor material Fabrication costs for compound semiconductor devices should decrease because larger substrates can be processed more economically and more readily compared to relatively smaller and more fragile conventional compound semiconductor wafers.

In the foregoing specification, the invention has been described with reference to specific embodiments.

However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. For example, use of Sb-based materials, such as indium antimonide (InSb), aluminum antimonide (AlSb), indium aluminum antimonide (InAlSb), gallium antimonide (GaSb), indium gallium antimonide (InGaSb), and aluminum gallium antimonide (InGaSb), is possible in accordance with the present invention. As those skilled in the art will appreciate, the present invention may be applicable to any heterojunction interband tunnel diode, resonant tunnel diode, or other tunnel diode structures in any III-V or compound semiconductor that can be lattice-matched to silicon using a perovskite or other appropriate oxide.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms ``comprises,'' ``comprising,'' or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A monolithic integrated circuit comprising:

an MOS circuit formed at least partially in a monocrystalline substrate;

a monocrystalline compound semiconductor layer overlying the monocrystalline substrate; and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer, the tunnel diode electrically coupled to the MOS circuit.

2. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a drain region and the tunnel diode is electrically coupled to the drain region.

3. The monolithic integrated circuit of claim 2 further comprising a second tunnel diode coupled to the drain region in series with the tunnel diode.

4. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a drain region and the tunnel diode is formed overlying and electrically coupled to the drain region.

5. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a gate electrode and the tunnel diode is formed overlying and electrically coupled to the gate electrode.

6. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises a digital circuit.

7. The monolithic integrated circuit of claim 1 wherein the tunnel diode comprises an interband tunnel diode.

8. The monolithic integrated circuit of claim 1 wherein the tunnel diode comprises an intraband tunnel diode.

9. A semiconductor device comprising:

a monocrystalline semiconductor substrate;

an oxide layer formed overlying the substrate;

a monocrystalline compound semiconductor layer formed overlying the oxide layer; and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer.

10. The semiconductor device of claim 9 wherein the tunnel diode comprises an intraband tunnel diode.

11. The semiconductor device of claim 10 wherein the tunnel diode comprises a quantum well layer sandwiched between first and second tunnel barrier layers and the first and second tunnel barrier layers are sandwiched between an injection layer and a collection layer.

12. The semiconductor device of claim 11 wherein the quantum well layer comprises GaAs and the first and second tunnel barrier layers comprise a material selected from AlGaAs and AlAs.

13. The semiconductor device of claim 12 wherein the quantum well layer and the first and second tunnel barrier layers are not intentionally doped.

14. The semiconductor device of claim 12 wherein the injection layer and the collection layer each comprise GaAs.

15. The semiconductor device of claim 14 wherein the injection layer and the collection layer are each impurity doped.

16. The semiconductor device of claim 15 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising monocrystalline GaAs more heavily impurity doped than the injection layer and the collection layer.

17. The semiconductor device of claim 12 further comprising a monocrystalline buffer layer interposed between the oxide layer and the monocrystalline compound semiconductor layer.

18. The semiconductor device of claim 17 wherein the oxide layer comprises an alkali earth metal titanate and the buffer layer comprises a material selected from the group consisting of GaAs and AlGaAs.

19. The semiconductor device of claim 18 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

20. The semiconductor device of claim 12 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

21. The semiconductor device of claim 20 wherein the substrate comprises silicon.

22. The semiconductor device of claim 21 further comprising a digital circuit formed at least partially within the substrate and coupled to the tunnel diode.

23. The semiconductor device of claim 11 wherein the quantum well layer comprises InGaAs and the first and second tunnel barrier layers comprise AlAs.

24. The semiconductor device of claim 23 wherein the injection layer and the collection layer each comprise InGaAs.

25. The semiconductor device of claim 24 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising heavily impurity doped monocrystalline InGaAs.

26. The semiconductor device of claim 24 further comprising a monocrystalline buffer layer between the oxide layer and the monocrystalline compound semiconductor layer.

27. The semiconductor device of claim 26 wherein the buffer layer comprises a material selected from the group consisting of InP and InAlAs.

28. The semiconductor device of claim 27 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

29. The semiconductor device of claim 9 wherein the oxide layer comprises an amorphous oxide layer.

30. The semiconductor device of claim 29 wherein the oxide layer comprises an amorphous oxide formed epitaxially as a monocrystalline oxide layer and subsequently heat treated to convert the monocrystalline oxide to an amorphous oxide.

31. The semiconductor device of claim 9 wherein the tunnel diode comprises an interband tunnel diode.

32. The semiconductor device of claim 31 wherein the tunnel diode comprises first and second quantum well layers spaced apart by a barrier layer and the first and second quantum well layers are sandwiched between first and second carrier supply layers.

33. The semiconductor device of claim 32 wherein the quantum well layers comprise InGaAs and the barrier layer comprises InAlAs.

34. The semiconductor device of claim 33 wherein the quantum well layers and the barrier layer are not intentionally doped.

35. The semiconductor device of claim 33 wherein the first carrier supply layers comprise a layer of n-doped InGaAs and a layer of n-doped InAlAs with the layer of n-doped InAlAs in contact with the first quantum well layer and the second carrier supply layers comprise a layer of p-doped InGaAs and a layer of p-doped InAlAs with the layer of p-doped InAlAs in contact with the second quantum well layer.

36. The semiconductor device of claim 35 further comprising a buffer layer comprising a material selected from the group consisting of InP and InAlAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

37. The semiconductor device of claim 36 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

38. The semiconductor device of claim 32 wherein the quantum well layers comprise InGaAs and the barrier layer comprises GaAs.

39. The semiconductor device of claim 33 wherein the first carrier supply layer comprises n-doped GaAs and the second carrier supply layer comprises p-doped GaAs.

40. The semiconductor device of claim 39 further comprising a buffer layer comprising GaAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

41. The semiconductor device of claim 39 wherein the oxide layer comprises an alkali earth metal titanate.

42. The semiconductor device of claim 41 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

43. The semiconductor device of claim 9 wherein the substrate comprises silicon.

44. The semiconductor device of claim 43 further comprising an amorphous silicon oxide formed underlying the oxide layer.

45. The semiconductor device of claim 9 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

46. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide, the monocrystalline compound semiconductor structure comprising an injection layer, a first tunnel barrier layer, a quantum well layer, a second tunnel barrier layer and a collection layer and

forming an intraband tunnel diode at least partially within the monocrystalline compound semiconductor structure.

47. The process of claim 46 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

48. The process of claim 47 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

49. The process of claim 46 wherein the step of growing a monocrystalline compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

50. The process of claim of claim 46 wherein the step of providing a semiconductor substrate comprises the step of providing a monocrystalline substrate comprising silicon.

51. The process of claim 50 further comprising the steps of:

forming a digital integrated circuit at least partially within the substrate; and

forming an interconnection electrically interconnecting the digital integrated circuit and the tunnel diode.

52. The process of claim 51 wherein the step of forming a digital integrated circuit comprises the step of forming an MOS transistor having a drain region at the surface of the substrate.

53. The process of claim 52 wherein the step of forming an interconnection comprises the steps of:

selectively ion implanting the layer of monocrystalline oxide overlying the drain region to render the oxide electrically conductive; and

forming the interband tunnel diode in electrical contact with the electrically conductive oxide.

54. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide, the monocrystalline compound semiconductor structure comprising a first carrier supply layer, a first quantum well layer, a barrier layer, a second quantum well layer, and a second carrier supply layer; and

forming an interband tunnel diode at least partially in the monocrystalline compound semiconductor structure.

55. The process of claim 54 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

56. The process of claim 55 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

57. The process of claim 54 wherein the step of growing a monocrystalline compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

58. The process of claim 54 further comprising the steps of:

forming a digital integrated circuit at least partially within the substrate; and

forming an interconnection electrically interconnecting the digital integrated circuit and the tunnel diode.

59. The process of claim 58 wherein the step of forming a digital integrated circuit comprises the step of forming an MOS transistor having a drain region at the surface of the substrate.

60. The process of claim 59 wherein the step of forming an interconnection comprises the steps of:

selectively ion implanting the layer of monocrystalline oxide overlying the drain region to render the oxide electrically conductive; and

forming the intraband tunnel diode in electrical contact with the electrically conductive oxide.

61. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline silicon substrate;

forming a CMOS circuit at least partially within the silicon substrate, the CMOS circuit comprising an MOS transistor having source and drain regions and a gate electrode;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

forming an amorphous layer of silicon oxide underlying the layer of monocrystalline oxide during the step of epitaxially growing;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide;

heat treating the layer of monocrystalline oxide to convert the monocrystalline oxide to an additional layer of amorphous oxide;

forming a tunnel diode at least partially from the monocrystalline compound semiconductor structure; and

forming an electrical interconnection between the tunnel diode and one of the source region, drain region and gate electrode.

62. The process of claim 61 wherein the step of epitaxially growing a layer of monocrystalline oxide comprises the step of epitaxially growing a layer of oxide selected from the group consisting of: alkali earth metal titanates, alkali earth metal hafnates, and alkali earth metal zirconates.

63. The process of claim 62 wherein the step of epitaxially growing a layer of monocrystalline oxide comprises the step of epitaxially growing a layer of $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

64. The process of claim 61 wherein the step of forming a tunnel diode comprises the step of etching the monocrystalline compound semiconductor structure to form the tunnel diode directly overlying the MOS transistor.

65. The process of claim 61 further comprising the step of forming a monocrystalline semiconductor buffer layer overlying the layer of monocrystalline oxide and underlying the monocrystalline compound semiconductor structure.

66. The process of claim 65 wherein the buffer layer comprises a material selected from InP, InAlAs, AlGaAs and GaAs.

HETEROJUNCTION TUNNELING DIODE AND PROCESS FOR FABRICATING THE SAME

Abstract of the Disclosure

High quality epitaxial layers of compound semiconductor materials can be grown overlying large silicon wafers by first growing an accommodating buffer layer on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer.

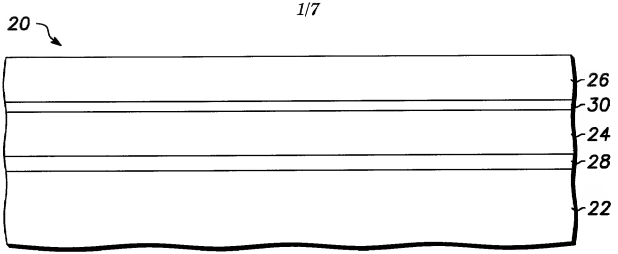


FIG. 1

FIG. 2

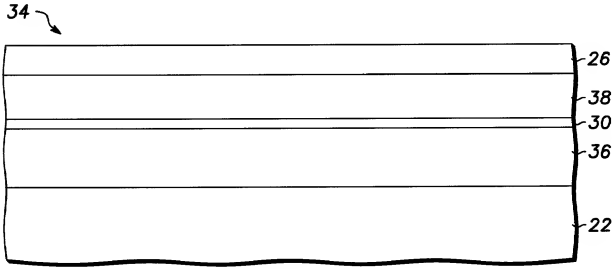


FIG. 3

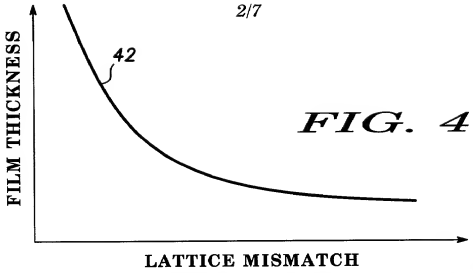


FIG. 4

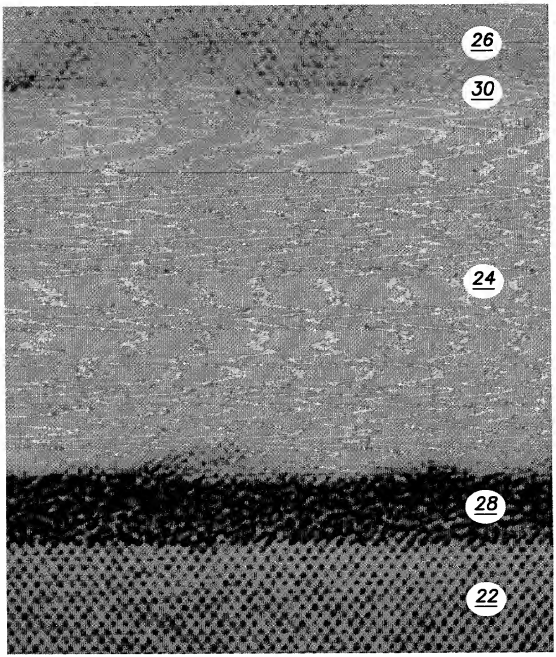
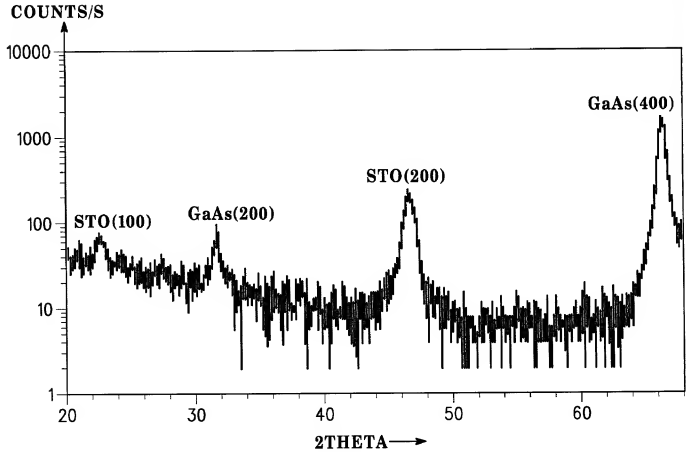


FIG. 5


COUNTS/S
10000
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GaAs(200)
STO(200)
GaAs(400)

FIG. 6

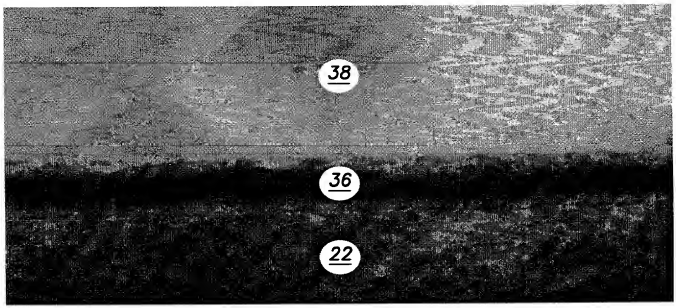
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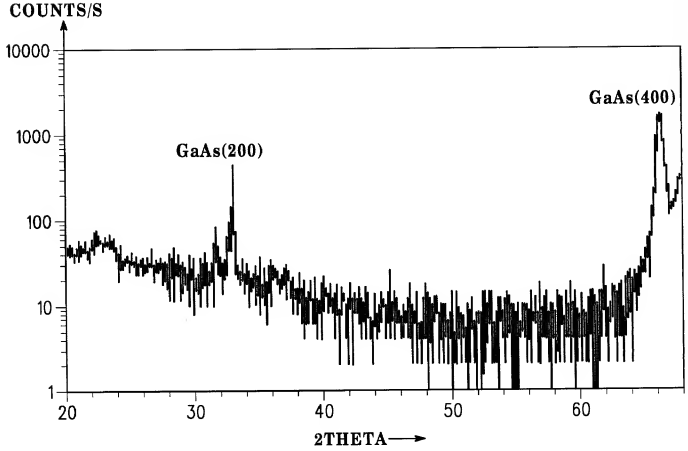
FIG. 7


COUNTS/S
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GaAs(400)
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FIG. 8

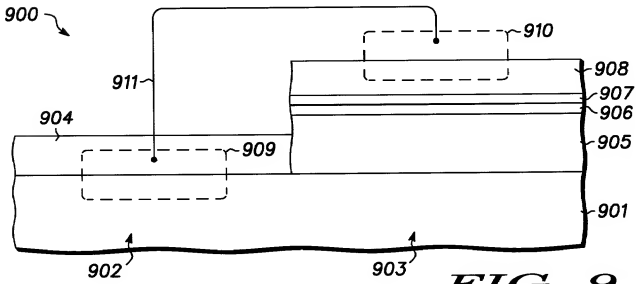
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FIG. 9

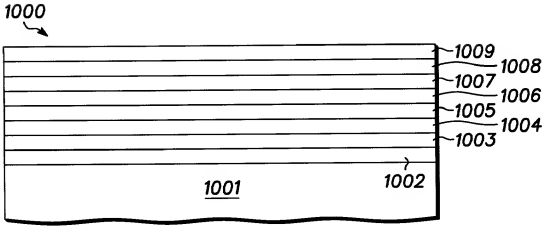

FIG. 10

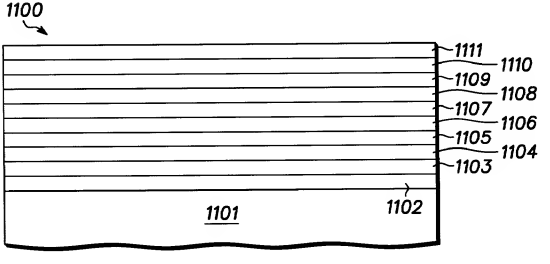

FIG. 11

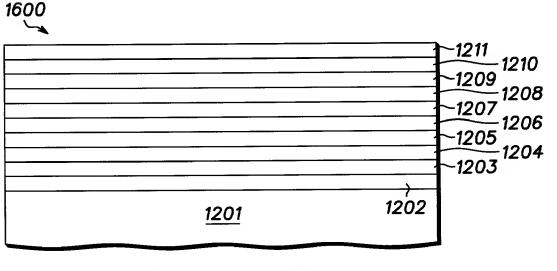

FIG. 12

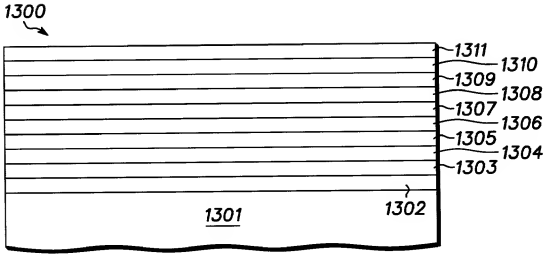
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FIG. 13

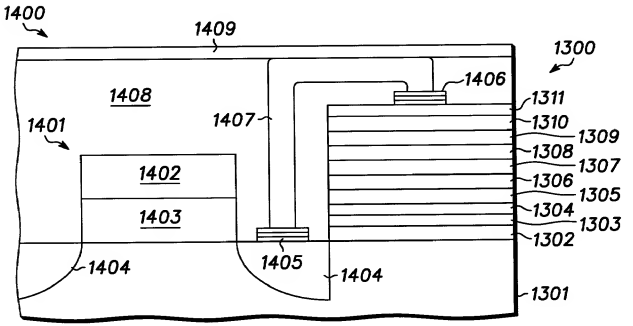
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FIG. 14

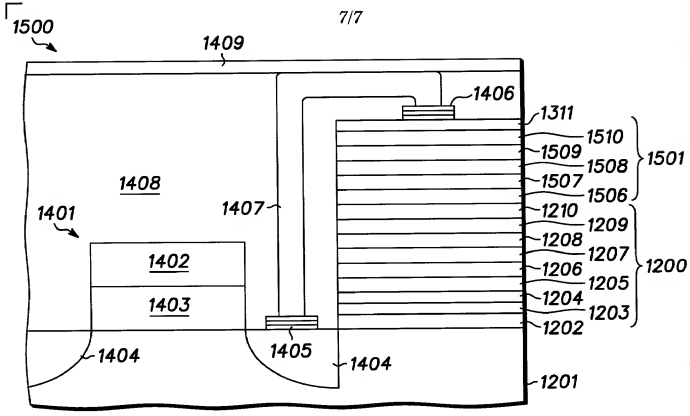

FIG. 15

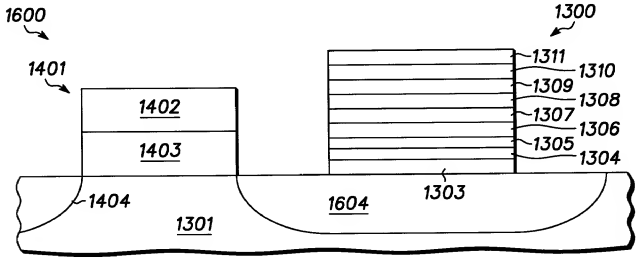

FIG. 16

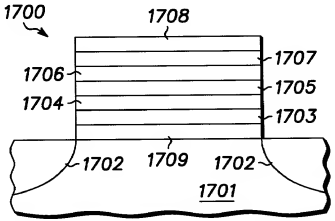

FIG. 17

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket JG00009

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled HETEROJUNCTION TUNNELING DIODES AND PROCESS FOR FABRICATING SAME, the specification of which is attached hereto unless the following box is checked:

☐ Application was filed on _____
as Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or 365(b) any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, § 119 of any United States provisional application(s), listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below:

(U.S. Parent Application Number or PCT Parent No.)	(Filing Date)	(Country)
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I hereby appoint the attorney(s) and/or agent(s) associated with Customer Number 23330 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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